

CLAIMS

What is claimed is:

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1. A transistor structure comprising:
2 a) a central channel region comprising a first semiconductor lightly doped
3 with a first impurity element to increase first conductivity free carriers;
4 b) a source region and a drain region on opposing sides of the central
5 channel region, both source region and the drain region being the first semiconductor
6 heavily doped with the first impurity element;
7 c) a gate adjacent the channel region and forming a junction with the
8 channel region, the gate comprising the first semiconductor and a second
9 semiconductor with an energy gap greater than the first semiconductor and being
10 doped with a second impurity element to increase carriers of the opposite
11 conductivity as the first free carriers.

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1. 2. The transistor structure of claim 1, further including a backgate adjacent the
2 channel region, and on an opposing side of the channel region from the gate, and
3 forming a junction with the channel region, the backgate comprising the first
4 semiconductor and a second semiconductor with an energy gap greater than the first
5 semiconductor and being doped with a second impurity element to increase carriers
6 of the opposite conductivity as the first free carriers.

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1. 3. The transistor structure of claim 2, wherein the fist semiconductor is silicon.

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1. 4. The transistor structure of claim 3, wherein the second semiconductor is
2 carbon and the first and second semiconductor form a silicon carbide crystal
3 structure.

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1. 5. The transistor structure of claim 4, wherein the first conductivity free carriers
2 are electrons and the second conductivity free carriers are holes.

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1 6. The transistor structure of claim 5, wherein the first impurity is arsenic.
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1 7. The transistor structure of claim 6, wherein the second impurity is boron.
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1 8. A silicon on insulator transistor structure comprising:
2 a) an insulating oxide layer separating a device layer of semiconductor
3 material from a bulk semiconductor base region;
4 b) a generally rectangular central channel region within the device layer
5 semiconductor material doped with a first impurity element to increase first
6 conductivity free carriers;
7 c) a source region and a drain region on opposing sides of the generally
8 rectangular central channel region, both the source region and the drain region
9 comprising the device layer semiconductor material heavily doped with the first
10 impurity element;
11 d) a gate adjacent the channel region and extending along a side of the
12 central channel region adjacent the source region and forming a junction with the
13 channel region, the gate comprising the device layer semiconductor and a second
14 semiconductor with an energy gap greater than the device layer semiconductor and
15 being doped with a second impurity element to increase carriers of the opposite
16 conductivity as the first free carriers.
17
1 9. The silicon on insulator transistor structure of claim 8, further including a
2 backgate adjacent the channel region, and on an opposing side of the channel
3 region from the gate, and forming a junction with the channel region, the backgate
4 comprising the device layer semiconductor and a second semiconductor with an
5 energy gap greater than the device layer semiconductor and being doped with a
6 second impurity element to increase carriers of the opposite conductivity as the first
7 free carriers.
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Sub A/H 1 10. The silicon on insulator transistor structure of claim 9, wherein the first
2 semiconductor is silicon.

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1 11. The silicon on insulator transistor structure of claim 10, wherein the second
2 semiconductor is carbon and the first and second semiconductor form a silicon
3 carbide crystal structure.

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1 12. The silicon on insulator transistor structure of claim 11, wherein the first
2 conductivity free carriers are electrons and the second conductivity free carriers are
3 holes.

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1 13. The silicon on insulator transistor structure of claim 12, wherein the first
2 impurity is arsenic.

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1 14. The silicon on insulator transistor structure of claim 13, wherein the second
2 impurity is boron.

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1 15. A method of controlling the flow of electricity between a source semiconductor
2 region and a drain semiconductor region, both heavily dopes with a first impurity
3 element, the method comprising:

4 a) positioning a generally rectangular central channel region between the
5 source region and the drain region, the channel region lightly doped with the first
6 impurity element to increase free carriers of a first type;

7 b) positioning a gate adjacent the channel region and extending along a
8 side of the central channel region adjacent the source region and forming a junction
9 with the channel region, the gate comprising the semiconductor and a second
10 semiconductor with an energy gap greater than the first semiconductor and being
11 doped with a second impurity element to increase free carriers opposite of the first
12 type; and

13 c) varying the potential of the gate region relative to the source region to
14 control depletion within the channel region.

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1 16. The method of controlling the flow of electricity of claim 15, further including:
2 d) positioning a backgate adjacent the channel region, and on an
3 opposing side of the channel region from the gate, and forming a junction with the
4 channel region, the backgate comprising the semiconductor and a second
5 semiconductor with an energy gap greater than the first semiconductor and being
6 doped with a second impurity element to increase free carriers opposite of the first
7 type; and

8 e) varying the potential of the backgate relative to the source region to
9 control depletion within the channel region.

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1 17. The method of controlling the flow of electricity of claim 16, wherein the fist
2 semiconductor is silicon.

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1 18. The method of controlling the flow of electricity of claim 17, wherein the
2 second semiconductor is carbon and the first and second semiconductor form a
3 silicon carbide crystal structure.

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1 19. The method of controlling the flow of electricity of claim 18, wherein the first
2 conductivity free carriers are electrons and the second conductivity free carriers are
3 holes.

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1 20. The method of controlling the flow of electricity of claim 19, wherein the first
2 impurity is arsenic.

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1 21. The method of controlling the flow of electricity of claim 20, wherein the
2 second impurity is boron.

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